Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A0**
2. **A1**
3. **A2**
4. **CS2**
5. **CS3**
6. **CS1**
7. **Y7**
8. **GND**
9. **Y6**
10. **Y5**
11. **Y4**
12. **Y3**
13. **Y2**
14. **Y1**
15. **Y0**
16. **VCC**

**.057”**

**.059”**

**14 13 12 11**

**4 5 6**

**15**

**16**

**1**

**2**

**3**

**10**

**9**

**8**

**7**

**MASK**

**REF**

**25138**

**14**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 25138**

**APPROVED BY: DK DIE SIZE .057” X .059” DATE: 7/11/22**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HC138**

**DG 10.1.2**

#### Rev B, 7/1